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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/753,852	01/08/2004	Marvin J. Rich	POU920030173US1	6046

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EXAMINER	
SIEK, VUTHE	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 03/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/753,852	RICH ET AL.	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/8/06*
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/753,852 filed on 1/8/2004. Claims 1-24 remain pending in the application.

Drawings

2. The drawings are objected to because the sheet of Fig. 2 filed on 2/27/04 does not include "Replacement Sheet" labeled as required. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities: related application information should be updated (see 0002, 0012, 0021, 0022, 0029).

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-2, 4, 7-8, 10, 13-14, 16, 19-20 and 22 are rejected under 35 U.S.C. 102(e) as being anticipated by Averbuj et al. (US 2005/0257109 A1).

6. As to claims 1, 7, 13 and 19, Averbuj et al. teach a method/system for testing integrated circuit (IC) (Figs. 1-6, summary) comprising a plurality of clock domains and at least on integrated chip, the method and system comprising a command transfer control hierarchy (Fig. 1 shows BIST Controller and Sequencers that hierarchically distribute and contribute commands) comprising a plurality of control levels (BIST controller at high-level and Sequencers at low-levels), including a first level comprising a master transfer control (BIST controller, 0028), and including at least one additional lower level (Sequencers, 0030), each lower level having a plurality of command transfer

controls configured serially, each command transfer control of a last level being associated with at least one of clock domains (0030); a communication protocol for communicating commands among the control levels (BIST controller communicates each of the algorithms to sequencers 8 [0029]; commands are distributed hierarchically through communications bus and memory interfaces, Fig. 1, 0031); and wherein command activation signals (CMD_REQ and SEQ_ACK, assert signal, Fig. 3, 0035-0038) are immediately propagated serially (sequentially) from the first level to lower levels and serially across command transfer controls in each level; (from BIST controller to Sequencers, algorithm controller 26 sequentially delivers each command to Sequencers 8, proceeds from one command to the next upon receiving an acknowledge signal from each of sequencers 8) and wherein command deactivation signal signals (CMD_REQ and SEQS_DONE, de-assert signal) are communicated serially among and across levels upon receipt of feedback from all lower levels that a command operation has been completed (algorithm controller 26 ensures that each sequencer has completed application of a current command to memory modules 12 via memory interfaces 10 before proceeding to the next command (Fig. 1, SEQS_DONE, Fig. 3, 0035-0038).

7. As to claims 2, 8, 14 and 20, Averbuj et al. teach the command transfer control hierarchy is scalable (BIST controller separates and distributes commands to sequencers according to command protocol, 0014).

8. As to claims 4, 10, 16 and 22, Averbuj et al. teach hierarchical self-test architecture (0046) (LBIST system).

Claim Rejections - 35 USC § 103

1. Claims 3, 5-6, 9, 11-12, 15, 17-18, 21 and 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Averhuj et al. (US 2005/0257109 A1) as applied to claims 1, 4, 7, 10, 13, 16, 19 and 22 above, and further in view of Ilyadis et al. (5,648,959).

2. As to claims 3, 5-6, 9, 11-12, 15, 17-18, 21 and 23-24, Averhuj et al. communication protocol as described above. Averhuj et al. does not teach communication protocol comprising a global synchronization signal. Ilyadis et al. teach timing synchronization is provided by a global synchronization mechanism in order to provide synchronization of serial data signals of all elements connected to the LAN Smarthub 10 in a communication protocol (col. 7 lines 23-26) (Fig. 1, item 58; Fig. 2, item 58; Fig. 7, item 236); Fig. 8 shows timing diagram of global synchronization signal and local synchronization signal, col. 4 lines 19-31; col. 4 lines 50-63; col. 6 lines 52-67; col. 7 lines 1-44). It would have been obvious to practitioners in the art to integrate a global synchronization mechanism including a global synchronization signal as taught by Ilyadis et al. in the communication protocol as taught by Averhuj et al. because the global synchronization mechanism provides a global synchronization signal to all elements interconnected to received serial data synchronized to the global clocks (col. 4 lines 50-63). Specifically by integrating a synchronization mechanism as taught by Ilyadis et al. into a communication protocol as taught by Averhuj et al. the serial data received by the memory modules operable at different clock domains would be

synchronized to global clock signals and the BIST controller (LBIST system) as taught by Averhuj et al. in Fig. 1 would be performed on clock domains synchronously and across the chips synchronously (clock domains of memory modules 12 are synchronized with BIST controller clock 4 (as global clock signal) across electronic device 2 in Fig. 1).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek

VUTHE SIEK
PRIMARY EXAMINER